LISTING OF THE CLAIMS:

1. (Currently Amended) A crack stop for an integrated circuit (IC) chip having an active circuit area, comprising:

the IC chip including a bottom substrate, metal layers separated by capping layers, a top aluminum layer, and copper or silver metal interconnects which do not form a self-passivating oxide layer, in a low-K dielectric material;

a moisture barrier/edge seal positioned along the outer peripheral edges of the active area of the IC chip;

a crack stop formed by at least one trench or void region outside of the moisture barrier/edge seal and between the moisture barrier/edge seal and ~~on~~ the outer periphery of the IC chip and extending substantially completely between the bottom substrate and the top aluminum layer of the IC chip, for preventing damage to the active area of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip during a dicing operation performed on the IC chip.

Claims 2 and 3 (Cancelled).

4. (Original) The crack stop for an IC chip as in claim 1, wherein the moisture barrier/edge seal comprises at least one inner boundary moisture barrier/edge seal formed by a metal stack around the active circuit area of the IC chip.

5. (Original) The crack stop for an IC chip as in claim 4, wherein each metal stack comprises a number of metal lines and via bars.

6. (Original) The crack stop for an IC chip as in claim 1, wherein the crack stop comprises a plurality of trenches or void regions formed outside of the moisture barrier/edge seal on the outer periphery of the IC chip.

7. (Currently Amended) A crack stop structure for preventing damage to an active area of an integrated circuit (IC) chip due to edge chipping and cracking from a dicing operation, comprising:

the active area of the IC chip comprising a bottom substrate, metal layers separated by capping layers, a top aluminum layer, and copper or silver interconnects which do not form a self-passivating oxide layer in a low K dielectric material;

a crack stop and a moisture barrier/edge seal, wherein the moisture barrier/edge seal comprises a metal stack extending around the active area of the chip, and the crack stop comprises a trench or groove outside of the moisture barrier/edge seal and between said moisture barrier/edge seal and ~~on~~ the outer periphery of the IC chip and extending substantially completely between the bottom substrate and the top aluminum layer of the IC chip~~, and the moisture/barrier edge seal comprises a metal stack between the crack stop and the active area of the chip~~.

8. (Withdrawn) A method for forming a crack stop for an integrated circuit (IC) chip having an active circuit area, wherein the IC chip includes metal interconnects which do not form a self-passivating oxide layer, in a low-K dielectric material, and a moisture barrier/edge seal positioned along the outer peripheral edges of the active area of the IC chip, at least one outer boundary crack stop formed by at least one trench or groove outside of the moisture

barrier/edge seal on the outer periphery of the IC chip for preventing damage to the active area of the IC chip caused by chipping and cracking formed along peripheral edges of the IC chip during a dicing operation performed on the wafer, the method comprising:

forming the IC chip on the wafer substantially to completion but without a final top aluminum Al layer;

forming the crack stop and the moisture barrier/edge seal by making a series of stacked via structures that form a boundary around the outer peripheral edges of the active area of the IC chip;

forming a top Al layer over the IC chip, without forming the Al layer on the regions of the crack stop, while forming the Al layer on the regions of the moisture barrier/edge seal, inside the perimeter of the crack stop, to protect the edge seal regions from a subsequent wet etch;

etching the wafer in a wet etch that removes the metal interconnect and barrier layers selective to Al, to form an etched out region as a crack stop.

9. (Withdrawn) The method of claim 8, including etching the wafer in a wet etch comprising dilute H2SO4:H2O2:HF.

10. (Withdrawn) The method of claim 8, including etching the wafer in a wet etch comprising dilute H2SO4:H2O2.

11. (Withdrawn) The method of claim 8, including forming the metal interconnects as copper interconnects.

12. (Withdrawn) The method of claim 8, including forming the metal interconnects as silver interconnects.

13. (Withdrawn) The method of claim 8, including forming the moisture barrier/edge seal by forming at least one inner boundary moisture barrier/edge seal by a metal stack around the active circuit area of the IC chip.

14. (Withdrawn) The method of claim 8, including forming each metal stack by forming a number of metal lines and via bars.

15. (Withdrawn) The method of claim 8, including forming at least one outer boundary crack stop as an etched out void region formed around the outer peripheral edges of the at least one inner boundary moisture barrier/edge seal.

16. (Previously Presented) An integrated circuit chip comprising:

a bottom silicon substrate;

a series of metal layers formed above the substrate, each of the metal layers including a low k dielectric material having a dielectric constant less than 4.0, and a copper interconnect, said metal layers defining an active circuit area of the integrated circuit chip;

a moisture barrier/edge seal forming an inner ring extending around the active circuit area of the integrated circuit, and consisting of a number of metal lines and via bars formed of copper;

a top aluminum layer covering said series of metal layers and forming two concentric ring-shaped openings; and

a crack stop forming an outer ring extending around the moisture barrier/edge seal, and consisting of a pair of etched out void regions located below the concentric ring-shaped openings of the top aluminum layer and on the outer periphery of the integrated circuit chip, said etched out void regions extending substantially completely between said top aluminum layer and said bottom substrate for preventing damage to the active area of the integrated circuit chip caused by chipping and cracking formed along peripheral edges of the integrated circuit chip during a dicing operation performed on the chip.

17. (Previously Presented) An integrated circuit according to Claim 16, wherein:

said etched out void regions are formed by a wet etch process;

said aluminum layer protects said moisture barrier/edge seal from said wet etch process; and

said metal interconnects do not form a self-passivating oxide layer.

18. (New) An integrated circuit according to Claim 17, wherein the crack stop extends outside of and around the moisture barrier/edge seal and between the moisture barrier/edge seal and an outside periphery of the IC Chip.